THE INVENTION CLAIMED IS:

1. A method for fabricating a stacked semiconductor package, comprising:
providing a substrate;
mounting a first semiconductor device on the substrate;
supporting an interposer above the first semiconductor device opposite the substrate;
electrically connecting the interposer to the substrate; and
mounting a second semiconductor device on the interposer.

2. The method of claim 1 further comprising partial mold encapsulating at least the first semiconductor device and at least a portion of the interposer to form an open cavity over the interposer.

3. The method of claim 1 wherein supporting the interposer further comprises:
supporting the interposer on a metallic stiffener having a plurality of legs contacting the substrate; and
supporting the metallic stiffener on the substrate.

4. The method of claim 3 further comprising forming at least one opening through the metallic stiffener for attaching at least one semiconductor device therethrough.

5. The method of claim 3 further comprising enhancing the stiffness of the metallic stiffener by connecting at least one pair of the legs with at least one base supporting member.

6. A method for fabricating a stacked semiconductor package, comprising:
providing a substrate;
mounting a first semiconductor device on the substrate;
supporting an interposer on a metallic stiffener above the first semiconductor device opposite the substrate;
electrically connecting the interposer to the substrate;
partial mold encapsulating at least the first semiconductor device and at least a portion of the interposer to form an open cavity over the interposer;
mounting a second semiconductor device on the interposer within the cavity; and
encapsulating the cavity with a top encapsulant.

7. The method of claim 6 wherein supporting the interposer on a metallic stiffener further comprises:

supporting the interposer on a metallic stiffener having:

a plane on which the interposer is supported; and

a plurality of legs extending from the plane and contacting the substrate; and

supporting the metallic stiffener on the substrate.

8. The method of claim 7 further comprising forming at least one opening through the plane for attaching at least one semiconductor device therethrough.

9. The method of claim 7 further comprising enhancing the stiffness of the metallic stiffener by connecting at least one pair of the legs opposite the plane with at least one base supporting member.

10. The method of claim 6 further comprising selecting the first and second semiconductor devices from at least one of a die, a flip chip die, a surface mountable passive, a multi-chip package, a fully assembled semiconductor package, a leadframe-based fully assembled semiconductor package, an array-based fully assembled semiconductor package, a system-in-a-package, and a combination thereof.

11. A stacked semiconductor package, comprising:

a substrate;

a first semiconductor device mounted on the substrate;

an interposer electrically connected to the substrate and supported above the first semiconductor device opposite the substrate; and

a second semiconductor device mounted on the interposer.

12. The stacked semiconductor package of claim 11 further comprising a partial mold encapsulant encapsulating at least the first semiconductor device and at least a portion of the interposer to form an open cavity over the interposer.

13. The stacked semiconductor package of claim 11 further comprising a metallic stiffener supporting the interposer, the metallic stiffener having a plurality of legs contacting the substrate and being supported thereon.

14. The stacked semiconductor package of claim 13 further comprising means forming at least one opening through the metallic stiffener for attaching at least one semiconductor device therethrough.

15. The stacked semiconductor package of claim 13 further comprising at least one base supporting member connecting at least one pair of the legs to enhance the stiffness of the metallic stiffener.

16. A stacked semiconductor package, comprising:

a substrate;

a first semiconductor device mounted on the substrate;

a metallic stiffener above the first semiconductor device opposite the substrate;

an interposer electrically connected to the substrate and supported on the metallic stiffener;

a partial mold encapsulant encapsulating at least the first semiconductor device and at least a portion of the interposer to form an open cavity over the interposer;

a second semiconductor device mounted on the interposer within the cavity; and

a top encapsulant encapsulating the cavity.

17. The stacked semiconductor package of claim 16 wherein the metallic stiffener has:

a plane supporting the interposer; and

a plurality of legs extending from the plane, contacting the substrate, and being supported thereon.

18. The stacked semiconductor package of claim 17 further comprising means forming at least one opening through the plane of the metallic stiffener for attaching at least one semiconductor device therethrough.

19. The stacked semiconductor package of claim 17 further comprising at least one base supporting member connecting at least one pair of the legs opposite the plane to enhance the stiffness of the metallic stiffener.

20. The stacked semiconductor package of claim 16 wherein the first and second semiconductor devices further comprise at least one of a die, a flip chip die, a surface mountable passive, a multi-chip package, a fully assembled semiconductor package, a leadframe-based fully assembled semiconductor package, an array-based fully assembled semiconductor package, a system-in-a-package, and a combination thereof.